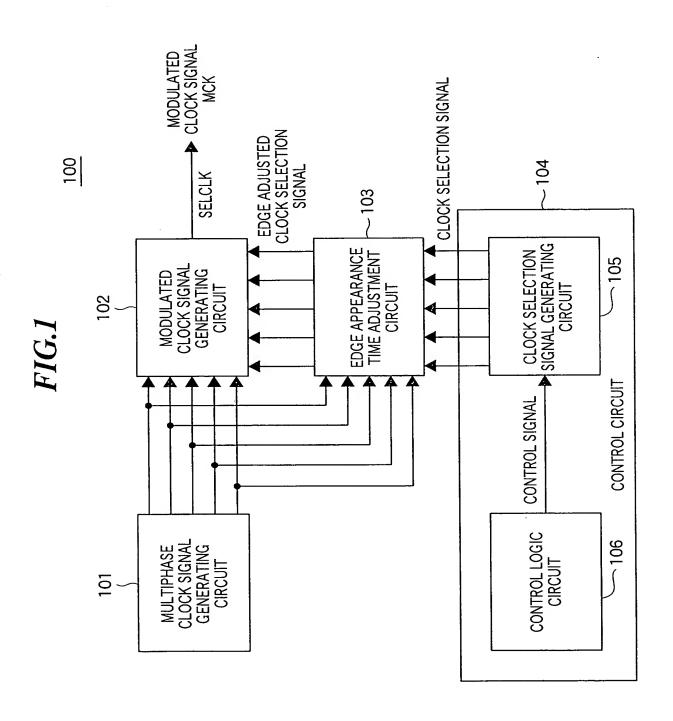
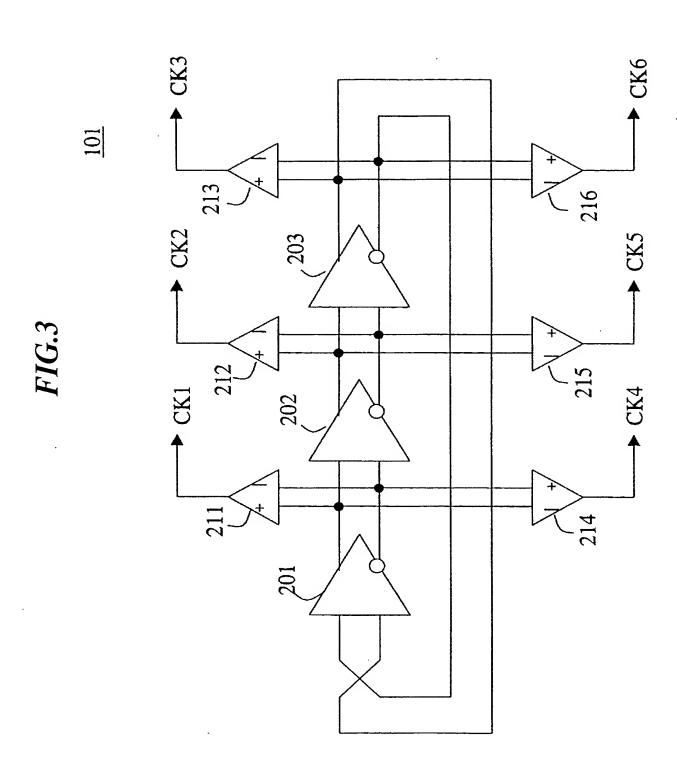
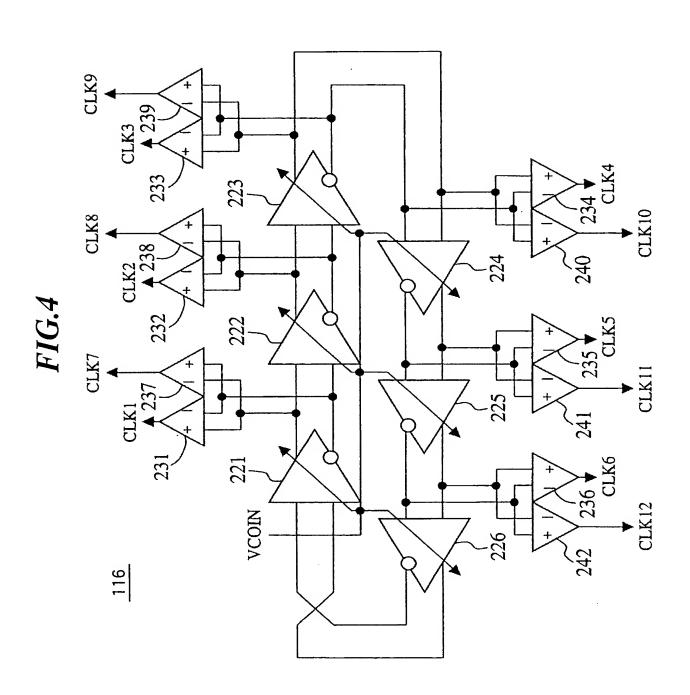
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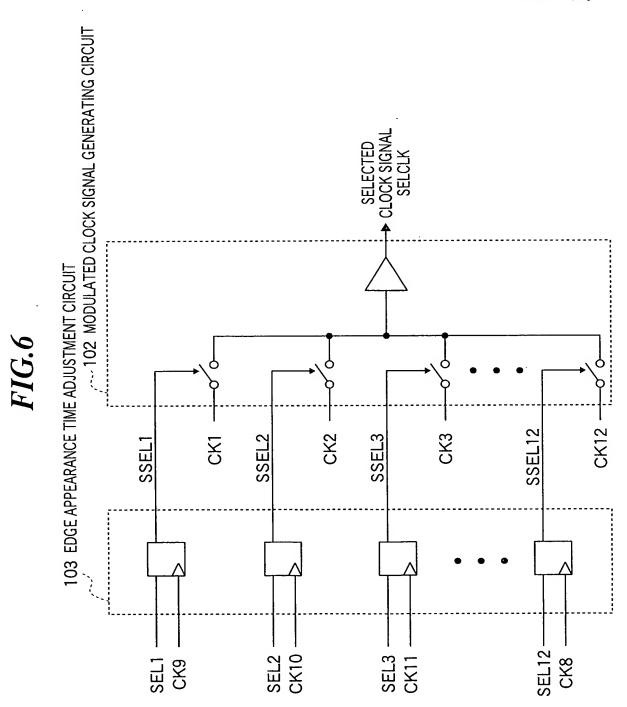
Seiichi OZAWA, et al PHASE-SELECTIVE TYPE FREQUENCY.... June 3, 2005 Alan. J. Kasper 202-293-7060 Q88132 2 of 22 2/22 537472 -SSEL1~12 MODULATED CLOCK SIGNAL 102 103 CLOCK SELECTION SIGNAL GENERATING EDGE APPEARANCE TIME ADJUSTMENT CIRCUIT MODULATED CLOCK SIGNAL GENERATING CIRCUIT DIVIDER 1/N SEL1~12··· CONTROL CIRCUIT CK1~12 CONTROL SIGNAL FIG.2 110 MULTIPHASE VCO CONTROL LOGIC CIRCUIT 116 106 104 SELECTED CLOCK SIGNAL H SELCLK PHASE COMPARISON CIRCUIT CHARGE DIVIDER 1/M DOWN 8 REFCLK -



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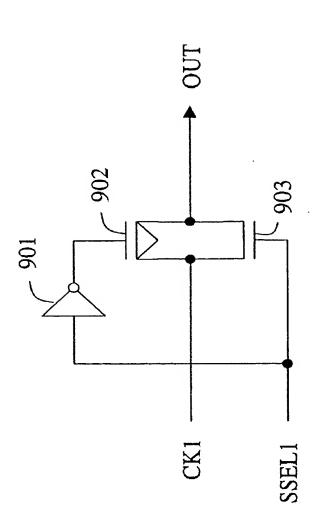


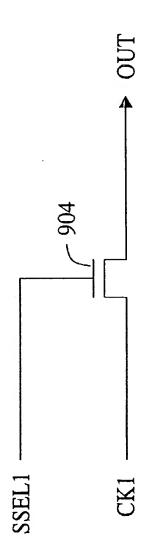
-- 102 MODULATED CLOCK SIGNAL GENERATING CIRCUIT 821 816 103 EDGE APPEARANCE TIME ADJUSTMENT CIRCUIT 811 SWITCH CIRCUIT ~815 \sim 814 SSEL6 ~813 SSEL5 ~812 SSEL4 806~ SSEL3 805~ SSEL 804~ SSEL1 803~ **CK3** CK4 CK5 CK2 SEL2 SEL5 SELG SEL3 SEL4



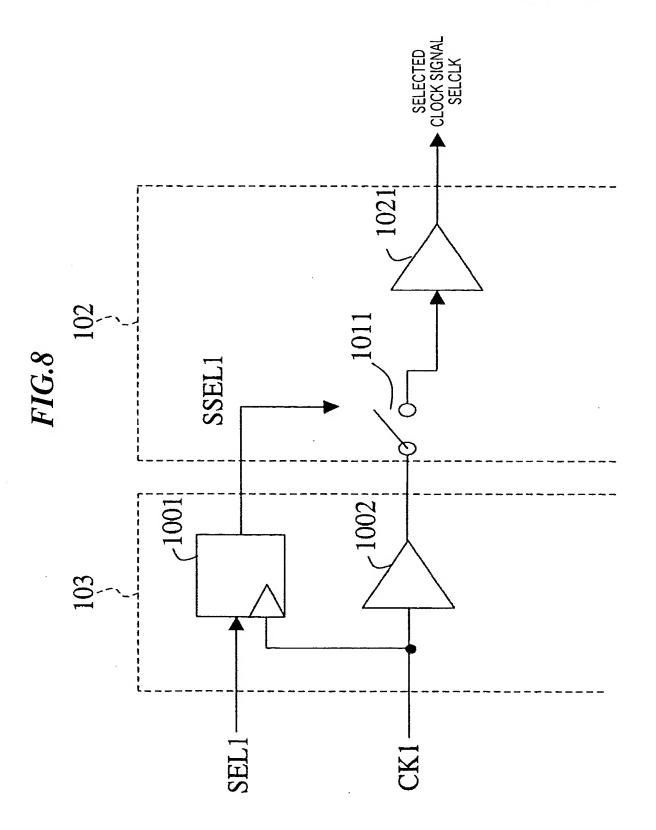
405. 1. A.

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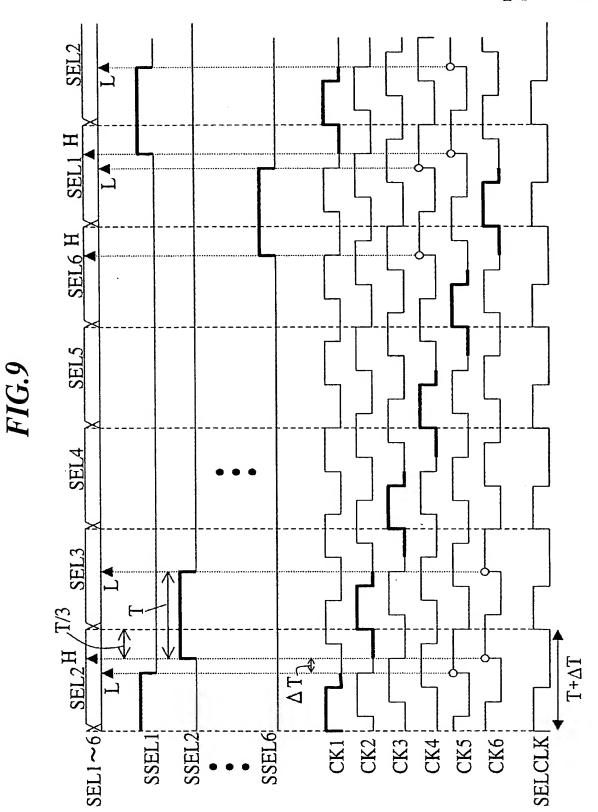


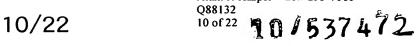


 $^{7}IG.7E$



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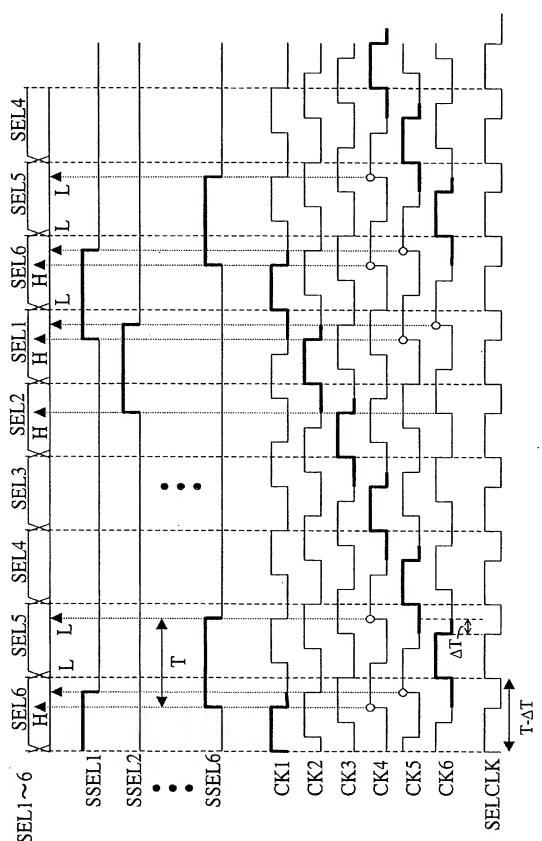


FIG.10

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-105 CLOCK SELECTION SIGNAL GENERATING CIRCUIT 104 ·CSG -603 -602 THREE-VALUED $\Delta \Sigma$ SELCLK FData ~106 CONTROL LOGIC CIRCUIT -601 FREQUENCY DATA GENERATOR

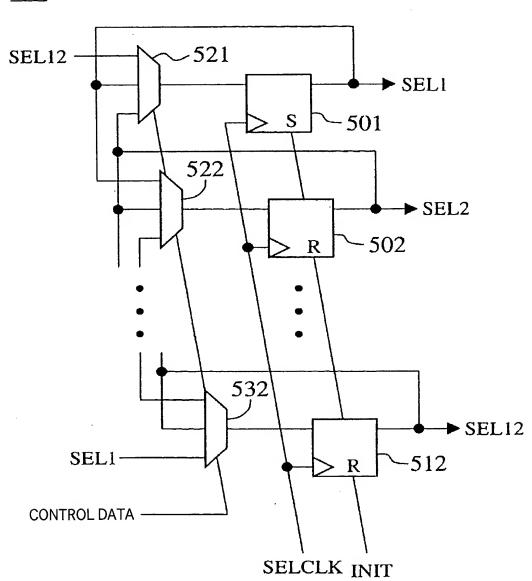
IG.II

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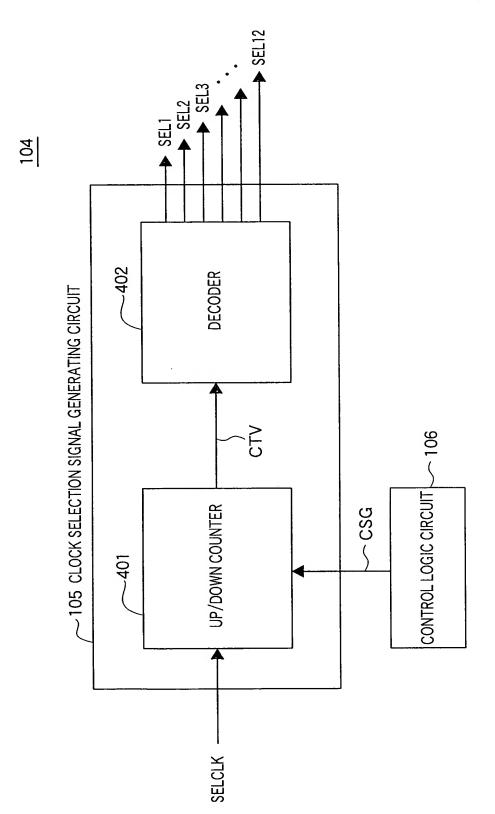
FIG.12

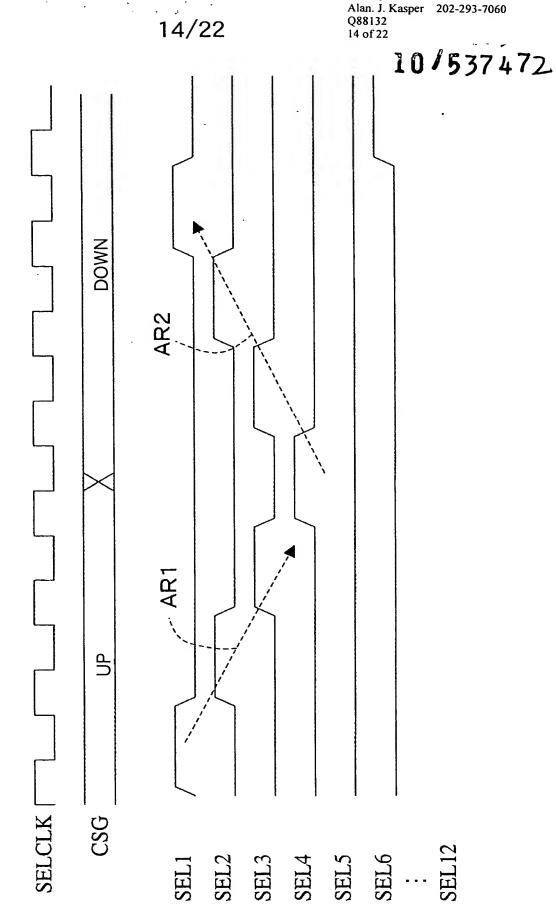
10/537472

<u>603</u>

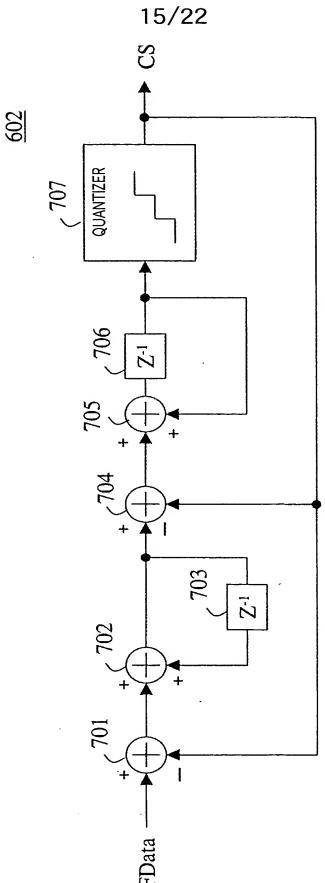


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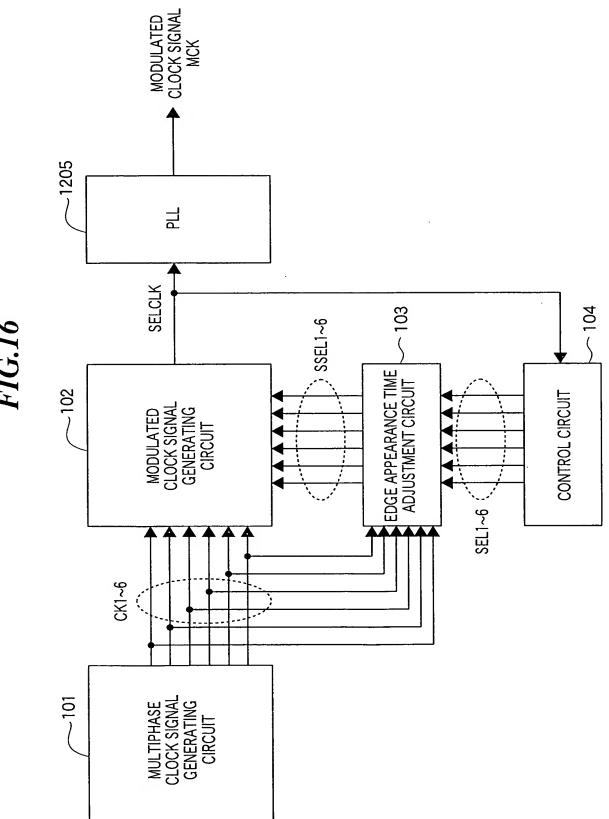
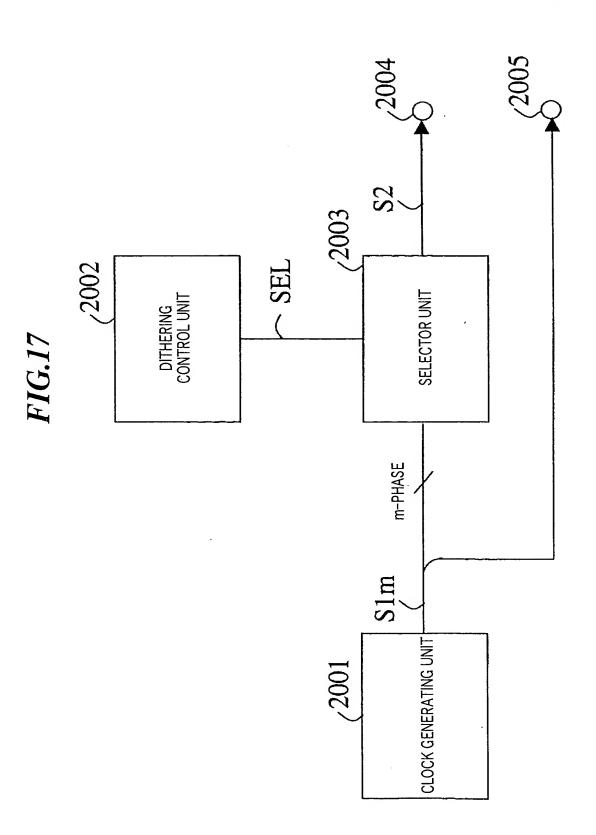
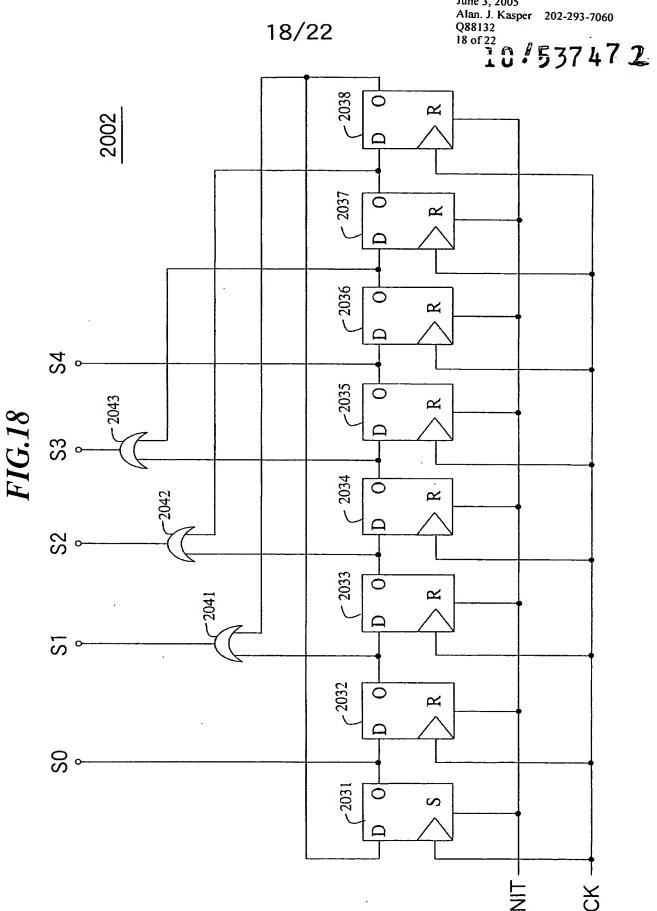


FIG.16





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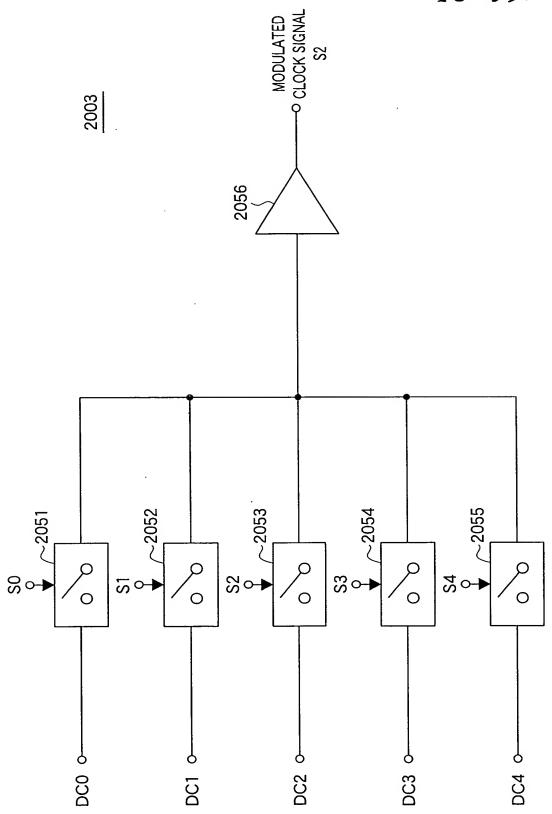
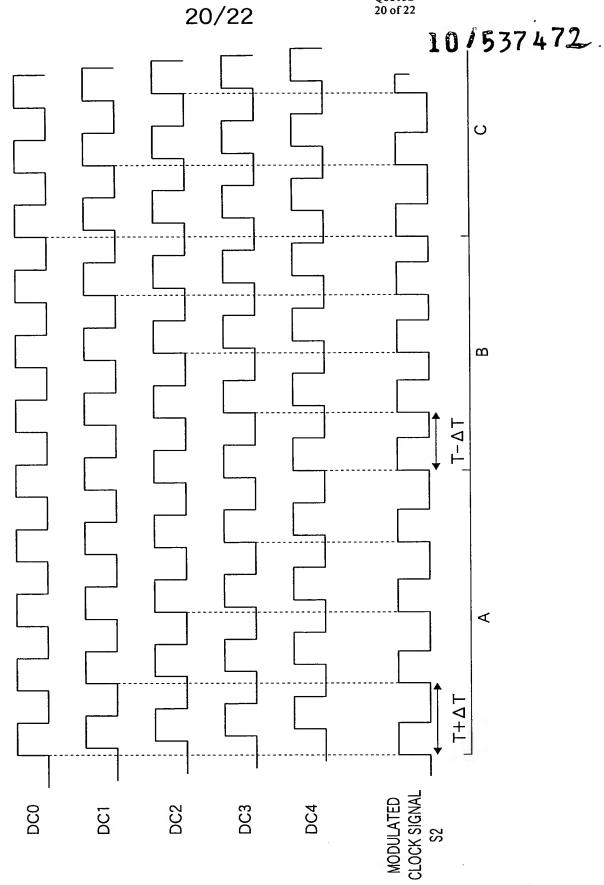


FIG.19

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FIG.21

